is shown, for example in Figure 7, wherein the transistors 66a and 70a must both conduct for the activation circuit 40a to trigger. See the specification at page 10, lines 15-21.

The objections to claim 11, with respect to antecedent basis, have been cured. The requirement that certain elements are essential is contraverted since there is no requirement that every element that is useful, functional, or operative in the circuit be claimed. In other words, there is no requirement in the patent law that the claim, in and of itself, recite a functional feature. M.P.E.P. 2172.01 simply requires that the claim make sense by reference to features. There is no need to detail the specific ways that are used in one embodiment claimed.

Therefore, reconsideration of the rejection is respectfully requested.

Claim 11 has been amended to be broadened in some respects and to include the limitation of claim 15, which was not rejected over the prior art. Therefore, claim 11 should now be in condition for allowance.

Claim 21 calls for a second circuit coupled to the first circuit to latch the first circuit in response to the power supply voltage being in a first state. While there is a latch in the cited reference, the latch does not function to latch a first circuit that develops a pulse indicating the power supply is not in its first state. In fact, it would appear that no such first circuit is connected to the latch and, therefore, cannot be latched by the latch.

On a similar analysis, the newly added claims should also patentably distinguish over the art of record.

Therefore, the application is now in condition for allowance, and the Examiner's prompt action in accordance therewith is respectfully requested.

Respectfully submitted,

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APPENDIX

Please cancel claims 1-10.

Please amend claim 11 as follows:

11 (Amended). An integrated circuit comprising:

an activation circuit to determine whether a supply voltage reaches a predetermined level;

a pulse generator to generate pulses to indicate that a supply voltage is ramping up and to terminate the generation of the pulses after the supply voltage reaches a predetermined level; and

[said activation circuit to prevent the pulses from being generated again, after the generation of the pulses has been terminated, until after the next power cycle] a feedback path to provide an output of said pulse generator to said activation circuit, said feedback path including an inverter to create a high signal in response to a low signal on said feedback path.

Please cancel claims 14 and 15.

Please amend claim 16 as follows:

16 (Amended). The integrated circuit of claim [15] 11 including a pair of transistors that must both conduct in order to generate said pulses.

Please add the following new claims 31 *et seq.*

31 (New). A method comprising:

developing a pulse indicating that a power supply voltage is not in a first state using a first circuit; and

latching the first circuit in response to the power supply voltage being in the first state using a second circuit.

32 (New). The method of claim 31 including latching the first circuit using the second circuit until the next power cycle.

33 (New). The method of claim 31 including using a logic functionality that emulates logic that is difficult to trigger.

34 (New). The method of claim 31 including detecting when a voltage is above at least two transistor threshold voltages using said second circuit to control said first circuit.

35 (New). The method of claim 31 including feeding back the output from the first circuit to the second circuit.

36 (New). The method of claim 35 including inverting the signal along said feedback path.

37 (New). The method of claim 36 including preventing the generation of said pulse unless a pair of transistors both conduct.

38 (New). The method of claim 37 including using a capacitor circuit to enable the supply voltage to reach a designated output level.

39 (New). The method of claim 38 including coupling a hysteresis sense stage to said capacitor circuit.

40 (New). A method comprising:

using an activation circuit to determine whether a supply voltage reaches a predetermined level;

generating pulses to indicate that a supply voltage is ramping up and to terminate the generation of pulses after the supply voltage reaches a predetermined level; and

providing an inverted output of said pulse generator to said activation circuit.

41 (New). The method of claim 40 including only generating a pulse when a pair of transistors both conduct.

42 (New). The method of claim 41 including using a capacitor circuit to enable the supply voltage to reach a designated output level.

43 (New). The method of claim 42 including using a hysteresis sense stage coupled to said capacitor circuit.